

INVENTIVE

cadence™

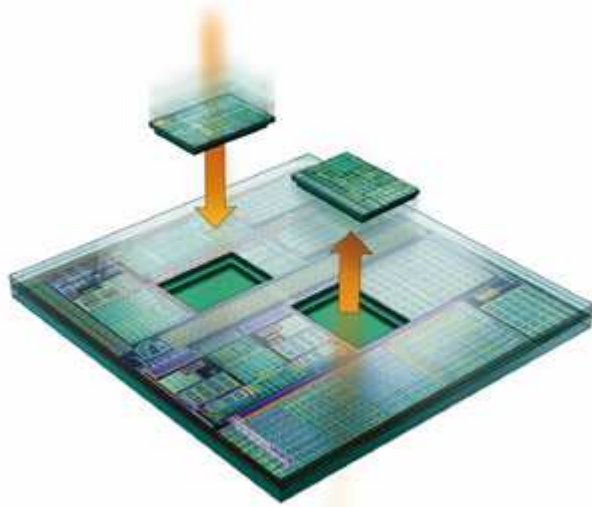
CONFIDENTIAL

65nm Design Issues

Y2010



Large scale, complex chip design



- **Previous large scale, complex chips**

- **Chip:** 1M instances, 500 pins, 20 Macros
- 90nm process technology
- 3 libraries and corners, 1 rc corner=3 runs

- **New large scale, complex chips**

- **Chip:** 5 - 20 blocks per chip
- **Blocks:** 1M-5M instances, 1000 pins, 100 macros
- 65nm, 45nm, 32nm process technology
- 3-5 libraries and 5-10 RC corners = 15-50 runs+

- **What it means for designers**

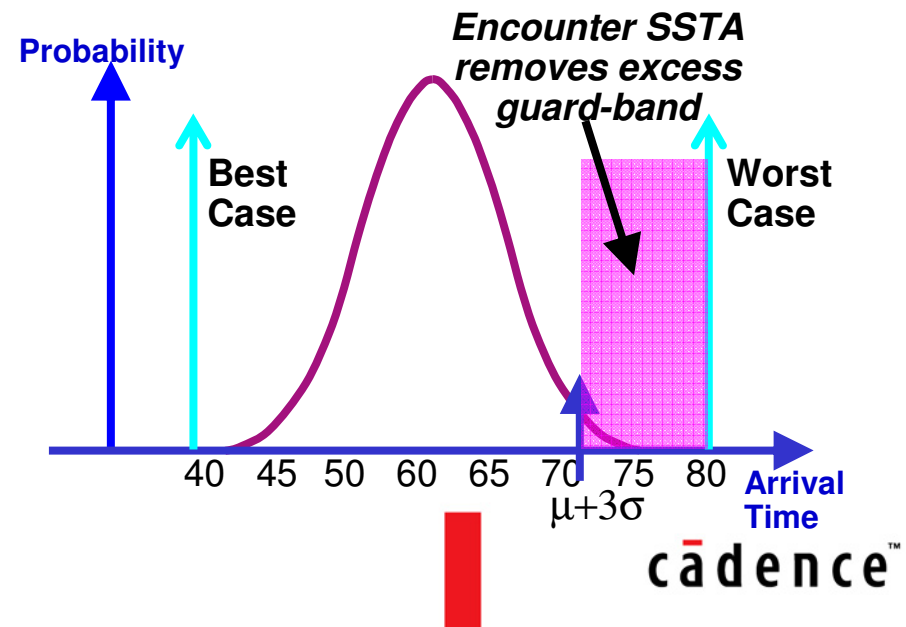
- 20+ floor plans for feasibility study
- Excessive runtimes due to big data
- More complex hierarchical designs
- Multi-dimensional timing closure

Process Variation

- Transistor & interconnect dimensions are shrinking rapidly
- Process control for small geometries is difficult
- Encounter Statistical STA (SSTA)
 - Accounts for variability of process parameters (ΔL , ΔW , ΔT_{ox} , etc.)
 - Eliminates need for multi-corner analysis & aggressive guard-band

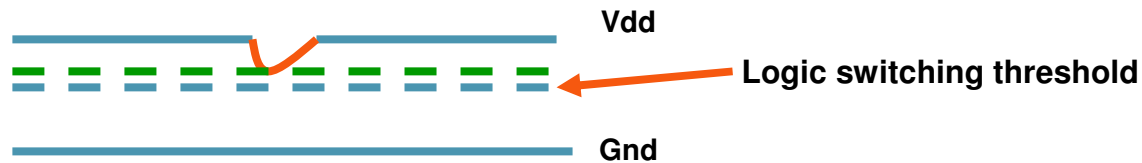
<u>Process A</u>	<u>Process B</u>
$L_{\text{mean}} = 1 \mu\text{m}$	$L_{\text{mean}} = 65 \text{ nm}$
$L_{\sigma} = 0.01 \mu\text{m}$	$L_{\sigma} = 0.01 \mu\text{m}$
<i>Delta-L of nominal = 1%</i>	<i>Delta-L of nominal = >15%</i>

Even if variability is constant between process generations, the net-effect gets worse

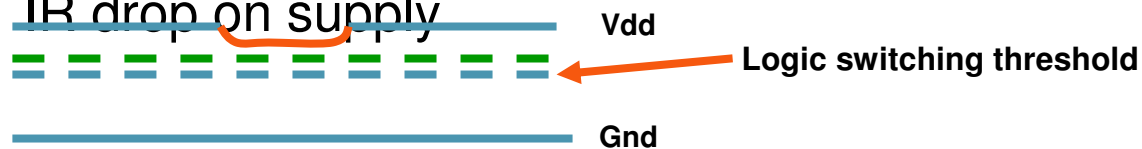


Impact of IR Drop on Noise

- Noise glitch without IR drop – No issue



- IR drop on supply



- Combined effect – Now the glitch might propagate.



- The combined effects can result in increased delays and nonfunctional circuitry due to weakened drivers and glitches crossing the logic switching threshold.

Power Tradeoffs with Traditional Methodologies

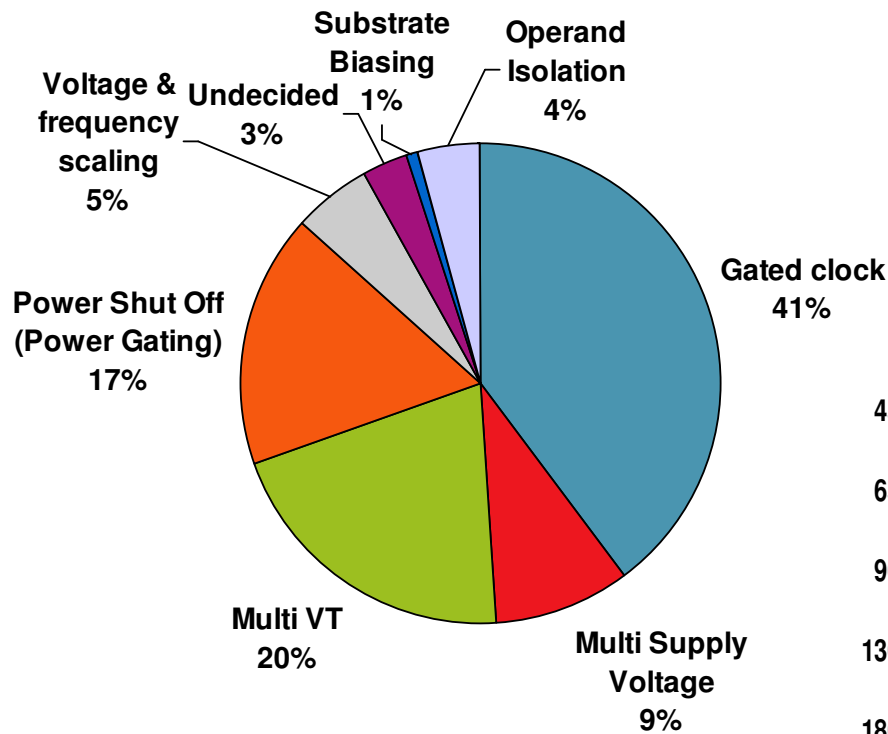
Power reduction technique	Power Savings	Timing penalty	Area penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Area optimization	Small	-None-	n/a	-None-	Low	-None-	Low
Multi-Vt optimization	Medium	Little	Little	-None-	Low	-None-	Low
Clock gating	Medium	Little	Little	-None-	Low	Low	Medium
Multi-supply voltage (MSV)	Large	Some	Little	High	Medium	Medium	High
Power shut-off (PSO)	Large	Some	Some	High	High	High	High
Dynamic & Adaptive Voltage Frequency Scaling (DVFS)	Large	Some	Some	High	High	High	High

Too Many Choices for Power Reduction, Too Hard to Decide

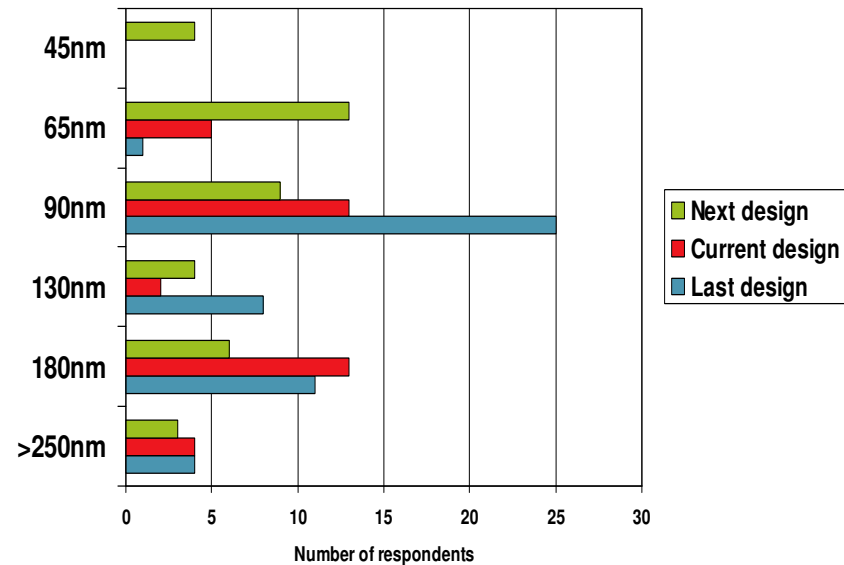
	Power reduction technique	Leakage power	Dynamic power	Timing penalty	Area penalty
Basic	Area optimization	1.1X	10%	0%	-10%
	Multi-Vt optimization	6X	0%	0%	2%
	Clock gating	0X	20%	0%	-10%to 2%
Advanced	Multi-supply voltage (MSV)	2X	40-50%	0%	<10%
	Power shut-off (PSO)	10-50X	~0%	4-8%	5-15%
	Dynamic and Adaptive Voltage Frequency Scaling (DVFS and AVS)	2-3X	40-70%	0%	<10%
	Substrate Biasing	10X	-	10%	<10%

Source – Customer interviews, Conference papers (ISSCC), magazine articles

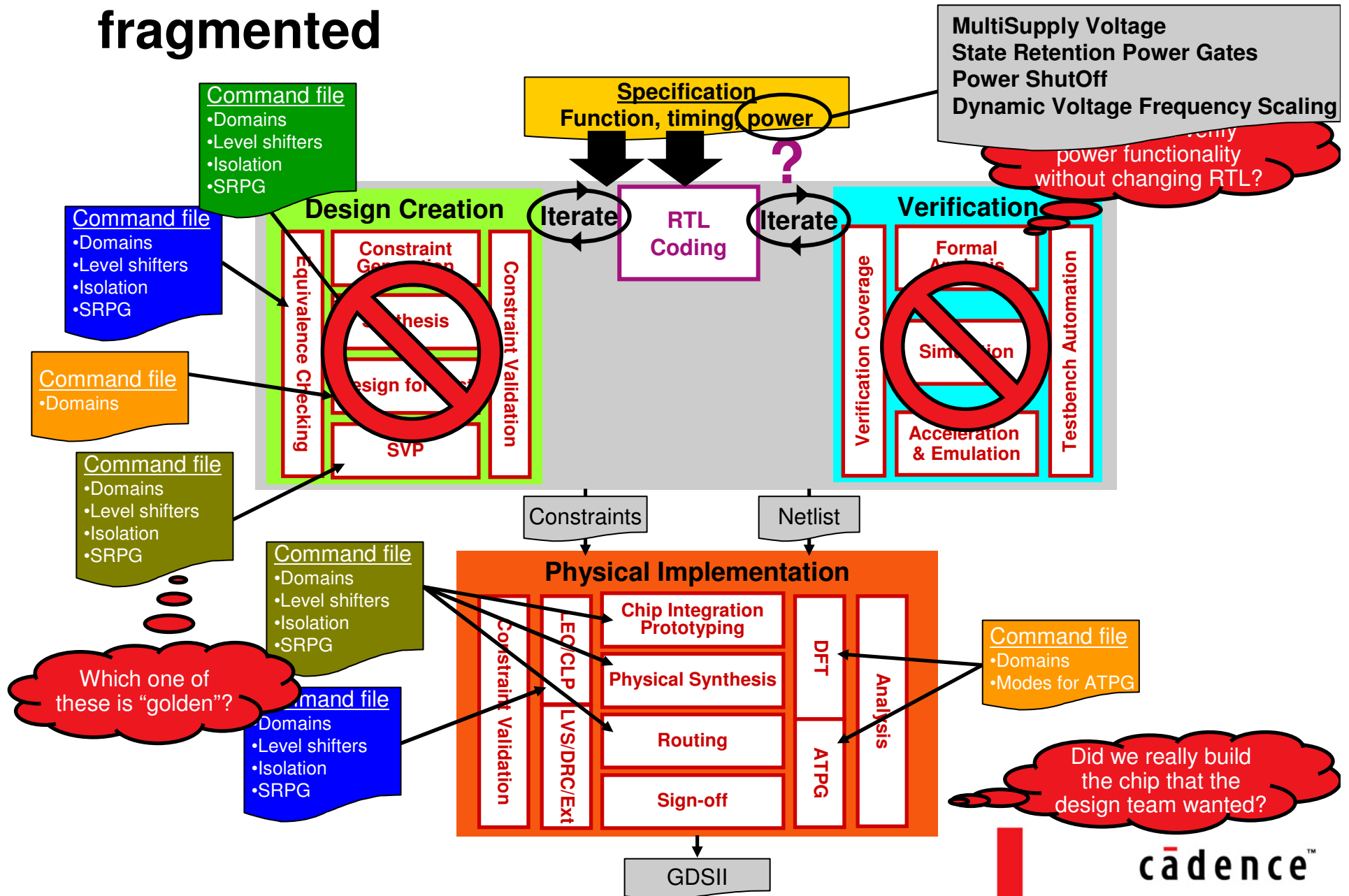
Low Power Techniques Used In Today's SoC



Source: 2007 Low Power workshop attendees survey

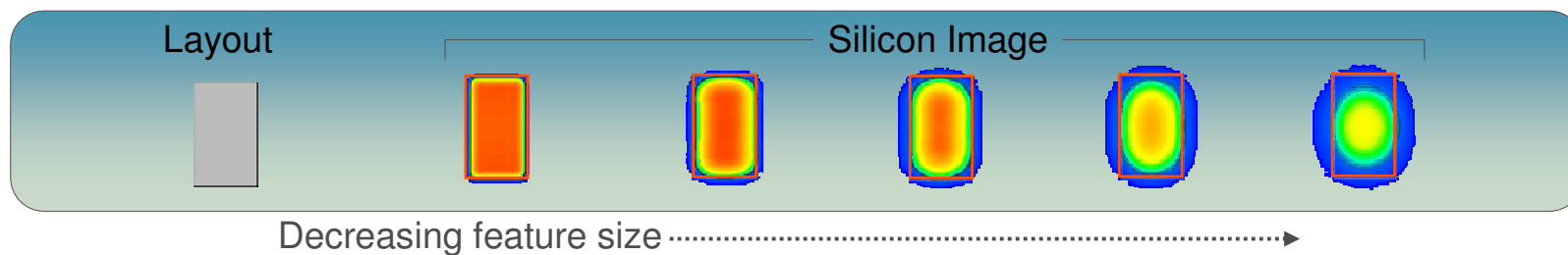
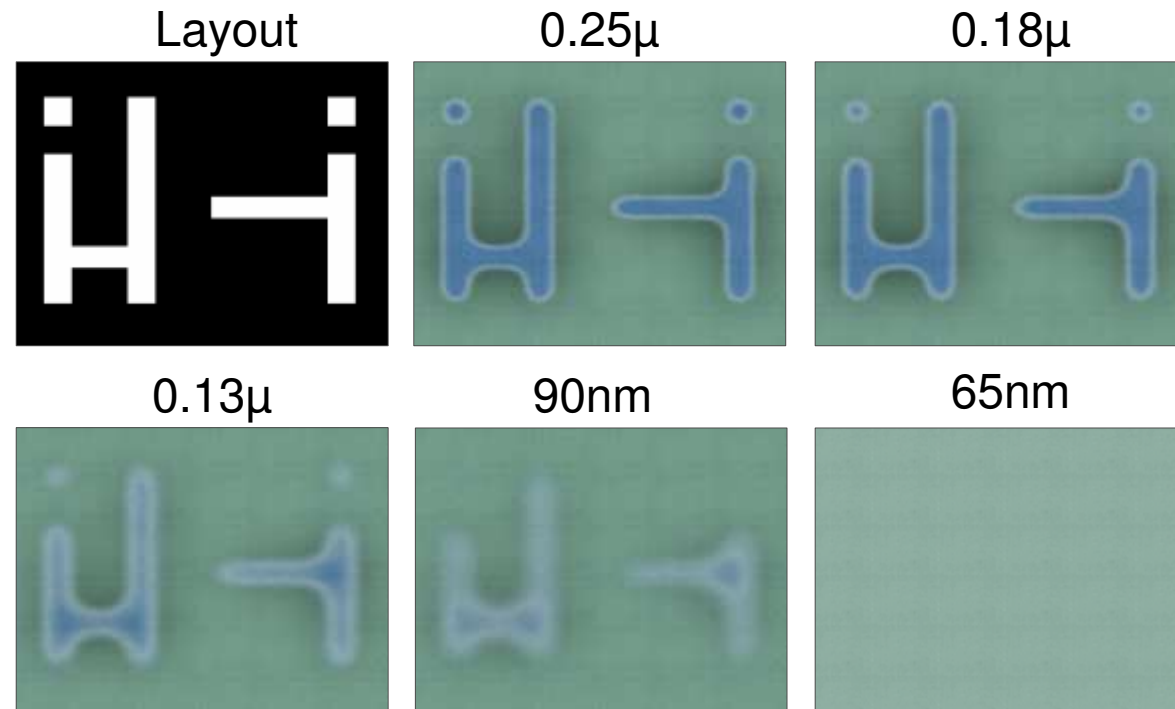


Current design-based solutions are fragmented



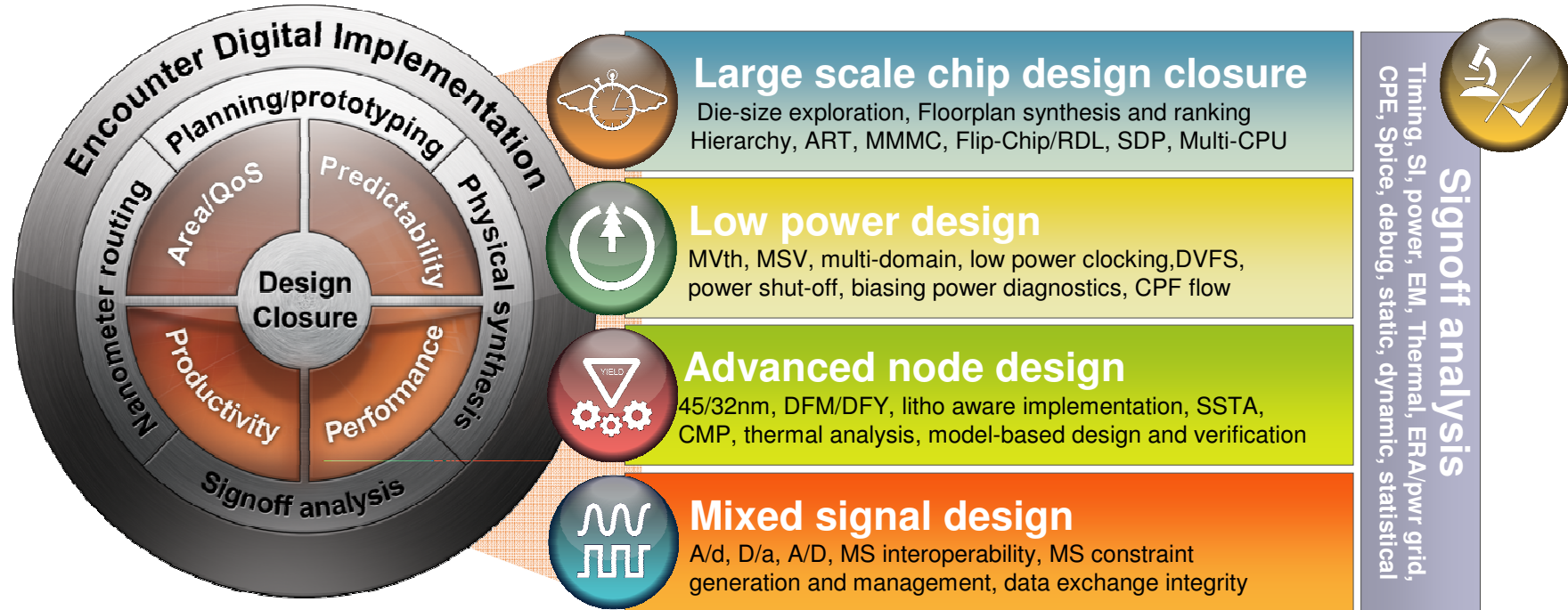
Manufacturability challenges

- 193nm wavelength of light for 65nm structures
Layout \neq printed
 - Bridging, necking, line end shortening
- Multiple objects contributes to the lithography effects



Encounter Digital Implementation System

Refining and redefining digital implementation



- Flexible, extensible design system
- End-to-end multi-core backplane
- Up to 60% power reduction
- 10-15% smaller die-size area
- New foundation memory architecture
- Automated advanced design flows
- Complete native MMMC flow
- Silicon accurate QoS (var/dfm/signoff)

Power Tradeoffs with A CPF-Based Methodology

Power reduction technique	Power Savings	Timing penalty	Area penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Area optimization	Small	-None-	n/a	-None-	Low	-None-	Low
Multi-Vt optimization	Medium	Little	Little	-None-	Low	-None-	Low
Clock gating	Medium	Little	Little	-None-	Low	Medium	Medium
Multi-supply voltage	Large	Some	Little	Medium	Medium	Medium	Medium
Power shut-off	Huge	Some	Some	Medium	Medium	Medium	Medium
Dynamic & Adaptive Voltage Frequency Scaling	Large	Some	Some	Medium	Medium	Medium	Medium

Cadence Low Power Solution



A Common Power Format Communicates the Power Intent Throughout the Flow

- **Common Power Format (CPF)** = Single specification of power intent used throughout design, verification, and implementation
- ASCII file that captures:

- **Power design intent**

- **Power domain**

- **Logical: hierarchical modules as domain members**
 - **Physical: power/ground nets and connectivity**
 - **Analysis view: timing library sets for power domains**

- **Power logic**

- **Level shifter logic**
 - **Isolation logic**
 - **State-retention logic**
 - **Switch logic & control signals**

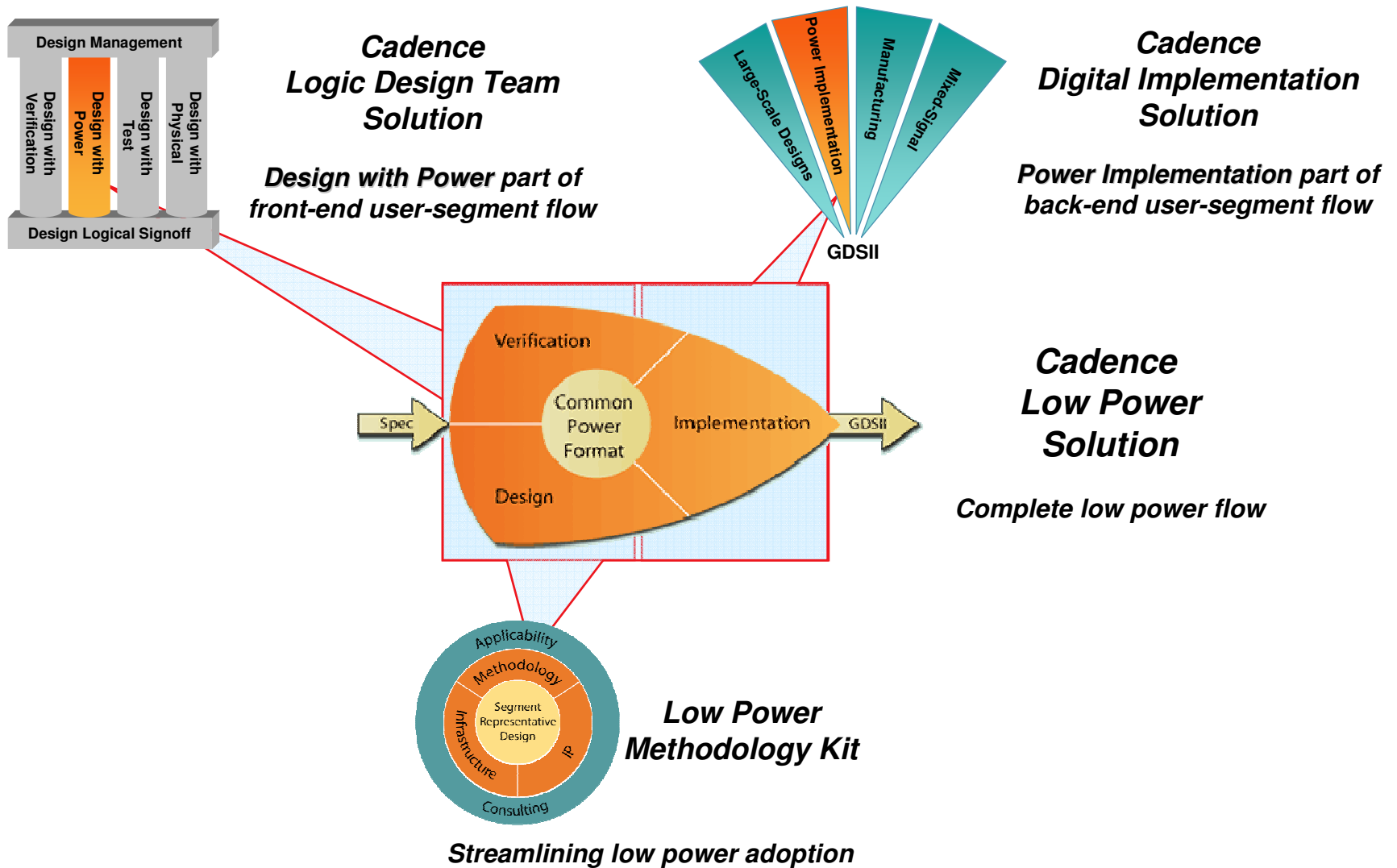
- **Power modes**

- **Definitions**
 - **Transition expressions**
 - **Modal analysis**

- **Technology information**

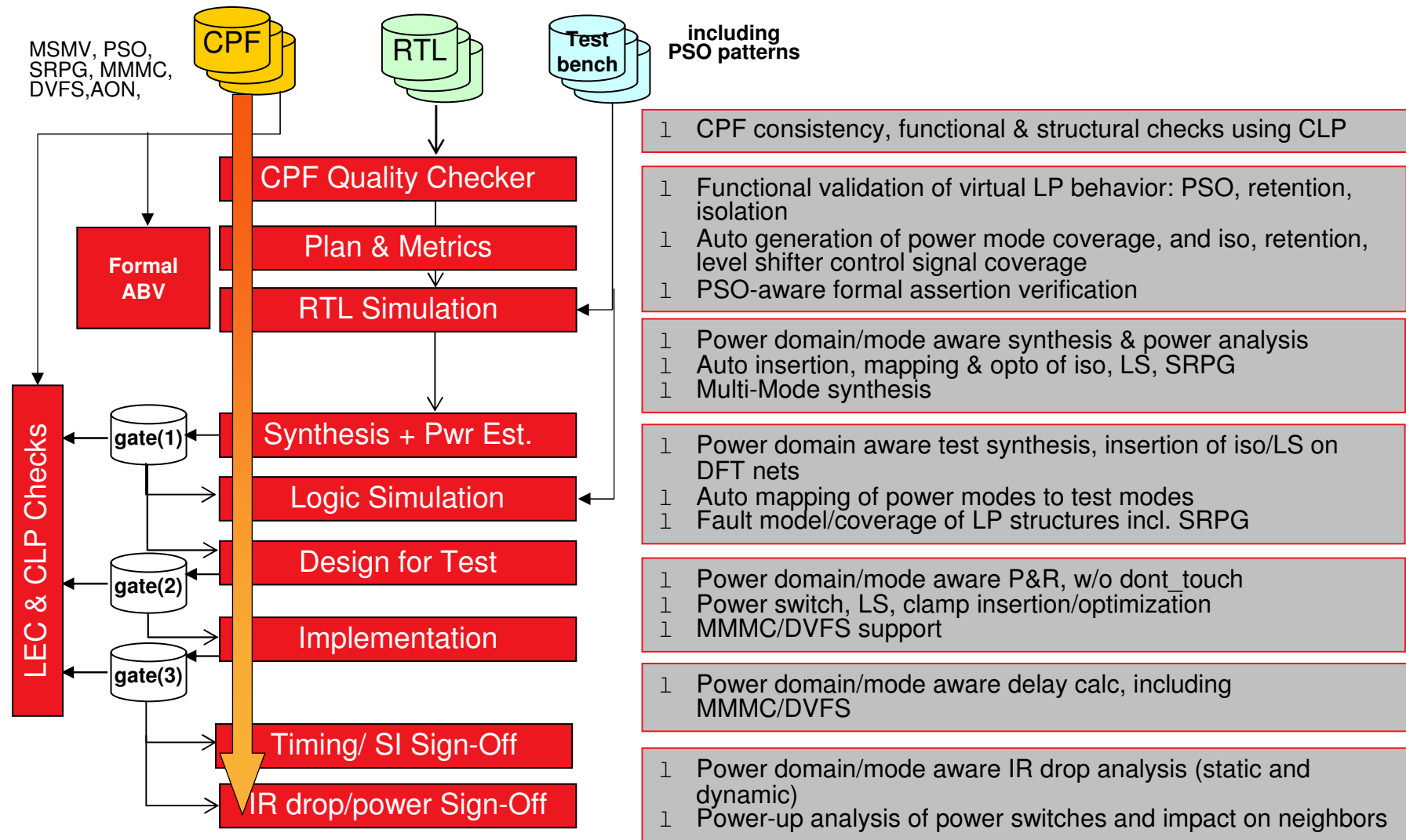
- **Level shifter cells**
 - **Isolation cells**
 - **State-retention cells**
 - **Switch cells**
 - **Always-on cells**

The Only Complete Low-Power Solution



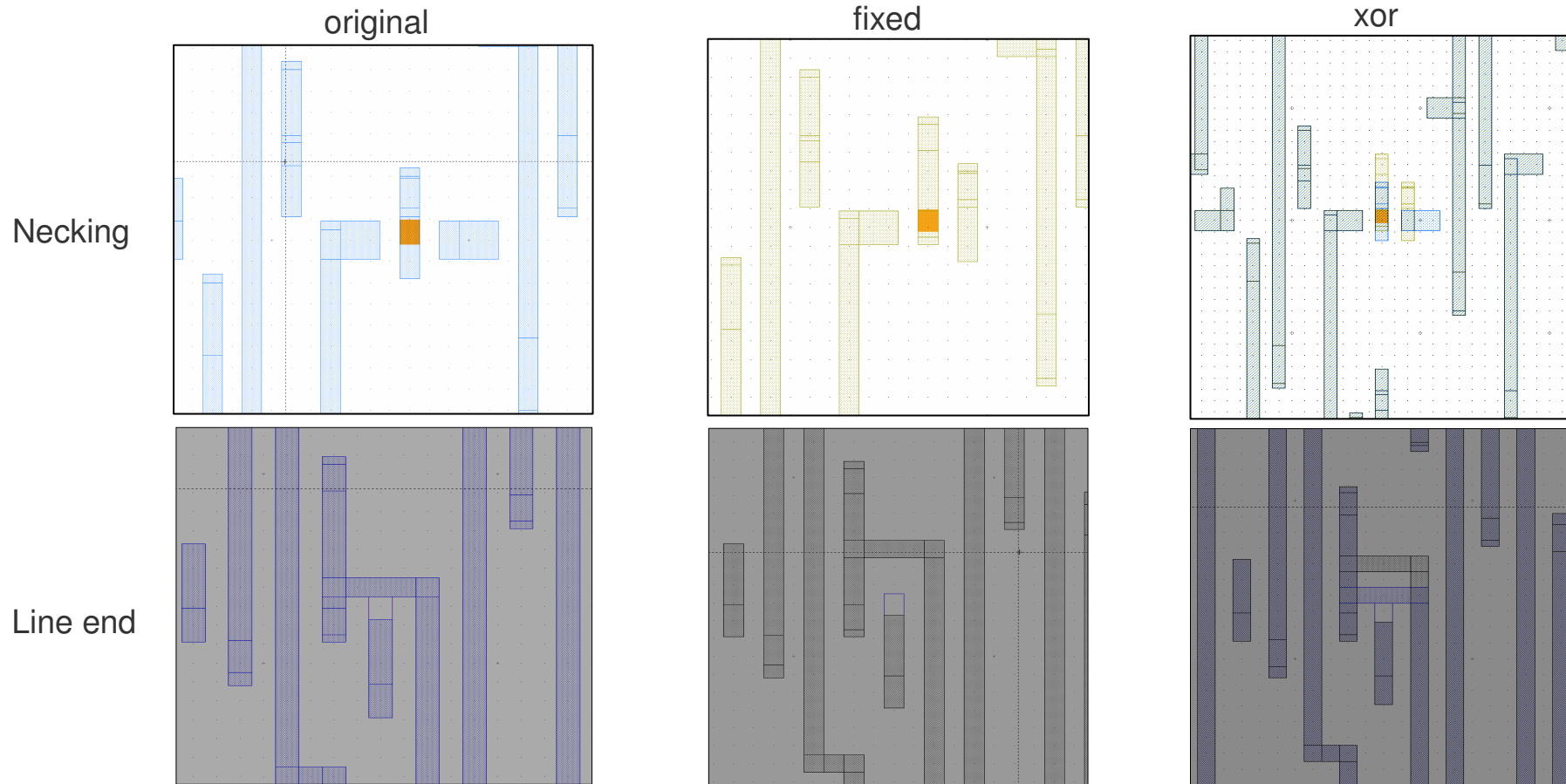
The CPF-Enabled Cadence Low Power solution

The Only Holistic Solution in the Market Today!



NanoRoute litho hotspot prevention

- Local area litho prevention/optimization
- No impact to timing and die size and no new hotspots



NanoRoute litho-driven routing

Patent pending

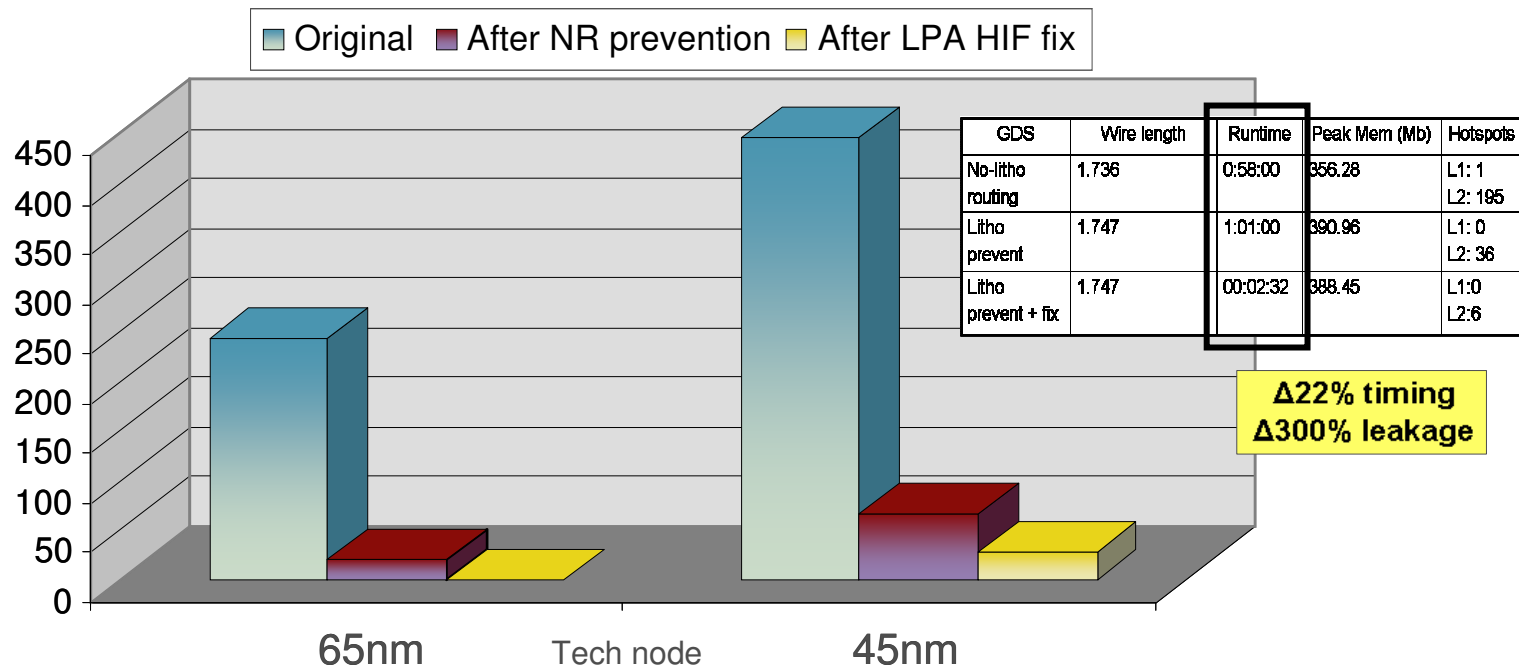
65nm node

- 1st iteration: >90% hot spots eliminated
- 2nd iteration: 100% hot spots eliminated

45nm node

- 1st iteration: >85% hot spots eliminated
- 2nd iteration: >94% hot spots eliminated

Hotspots @ +/-20nm defocus and +/-5% dose



Machine used: Linux 2 2.19GHz CPU. 16G memory.

Large scale chip design solution

Enabling the largest, most complex designs

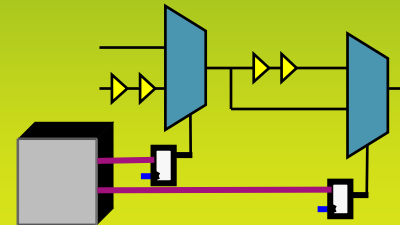
Faster
time to market
Better
quality of silicon

- Full chip prototyping
- Design exploration
- Floorplan synthesis
- Die size reduction

Planning/Prototype

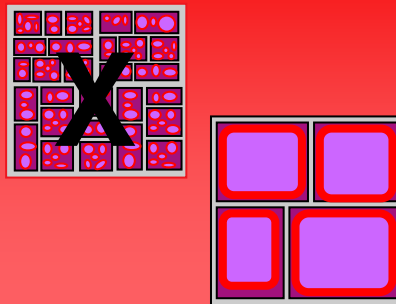


QoS closure



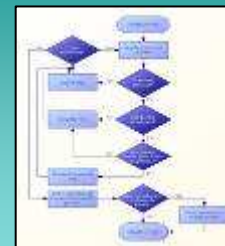
- In-system signoff
- Early rail analysis
- SMART routing
- Multi-objective opt

Scalability



- Active logic Reduction Technique (ART)
- New foundational memory architecture
- Multi-CPU backplane

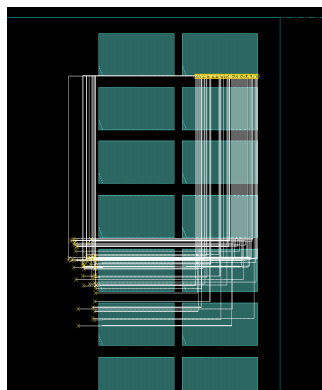
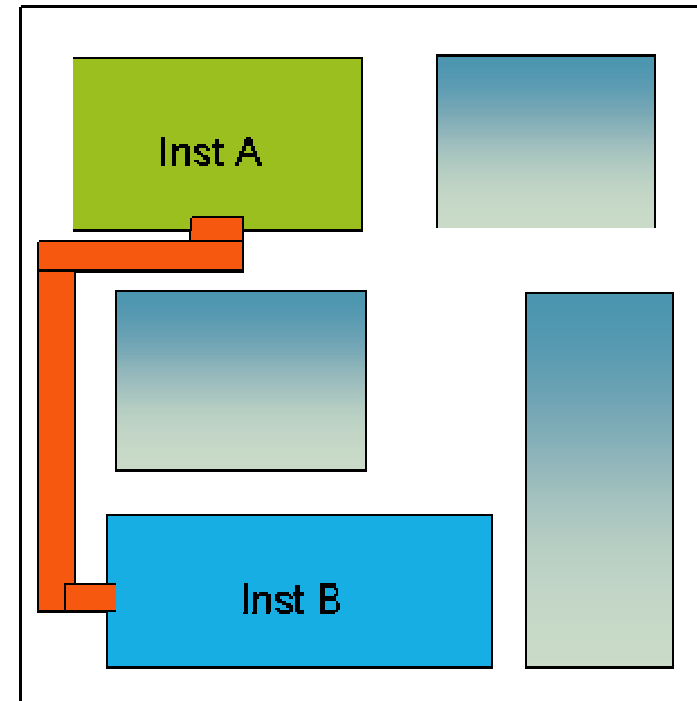
Complexity



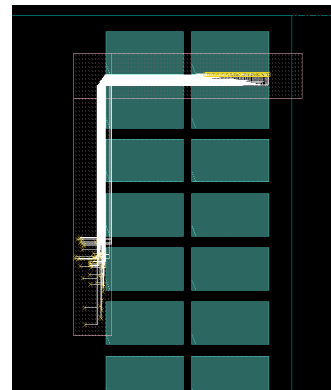
- Full flow MMMC
- Variation and DFM aware
- Post-mask ECO flow
- Flip-Chip/RDL design

Bus routing guides

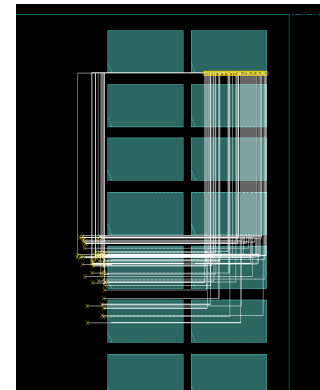
- Bus guides are floorplan objects to guide routing/pins for selected nets
- Specify layer or layer range
 - Routing outside bus guides has higher cost
 - Warning issued if routing is outside bus guides



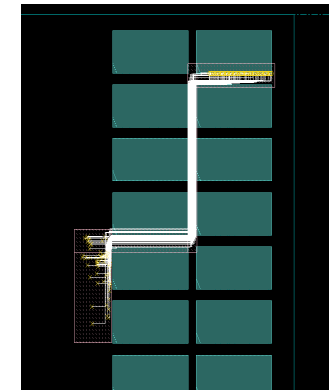
No bus guides



Using guides



No bus guides



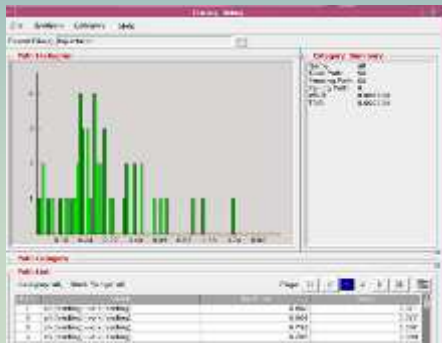
Using guides

Global debug and diagnostics

- Integrated and complete diagnostics
- Intuitive, easy to use, graphical/visual/report based

Global Timing Debug

- Available since 2006
- Failed path/constraint checking and optimization
- Detailed path analysis
- Cross-probing with phys
- MMMC analysis/debug



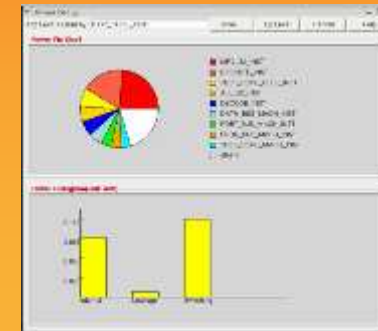
Global Clock Debug

- Visually check/debug clock
- Instance and path finding
- Cross-probing physical/log
- Expand/collapse clks for hierarchical viewing



Global Power Debug


- Complete power debug
- Diagnose top consuming nets, consumption by hier, domain, instance, clks...
- What-if analysis and opt
- Uses signoff engines

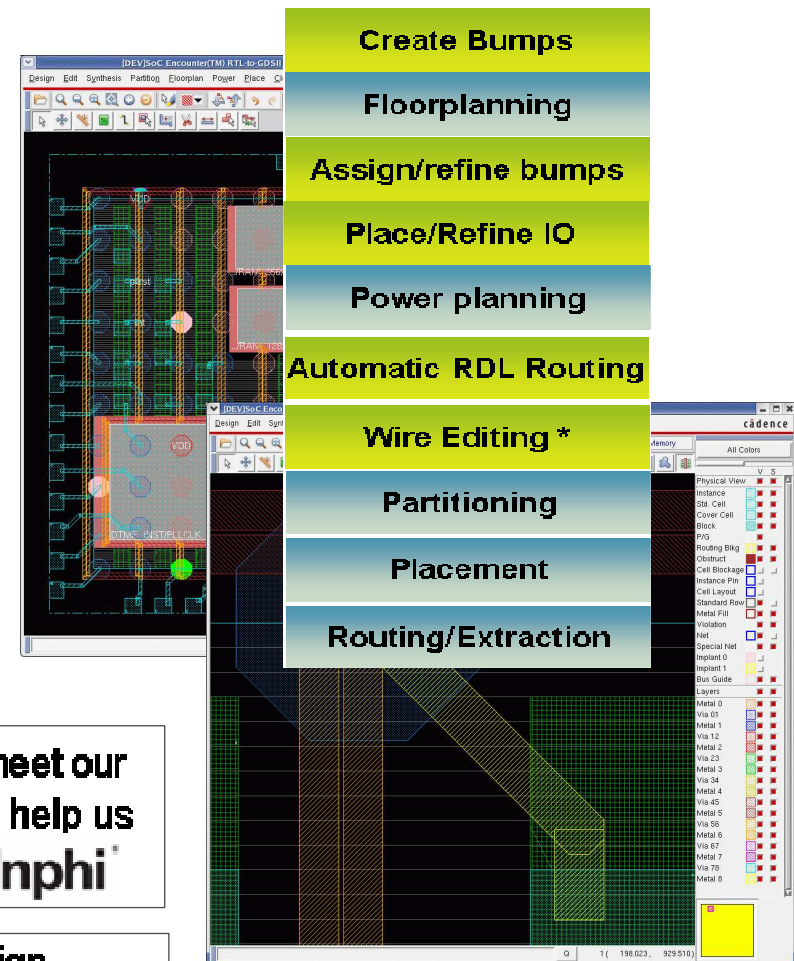


Package aware IO planning and flip-chip

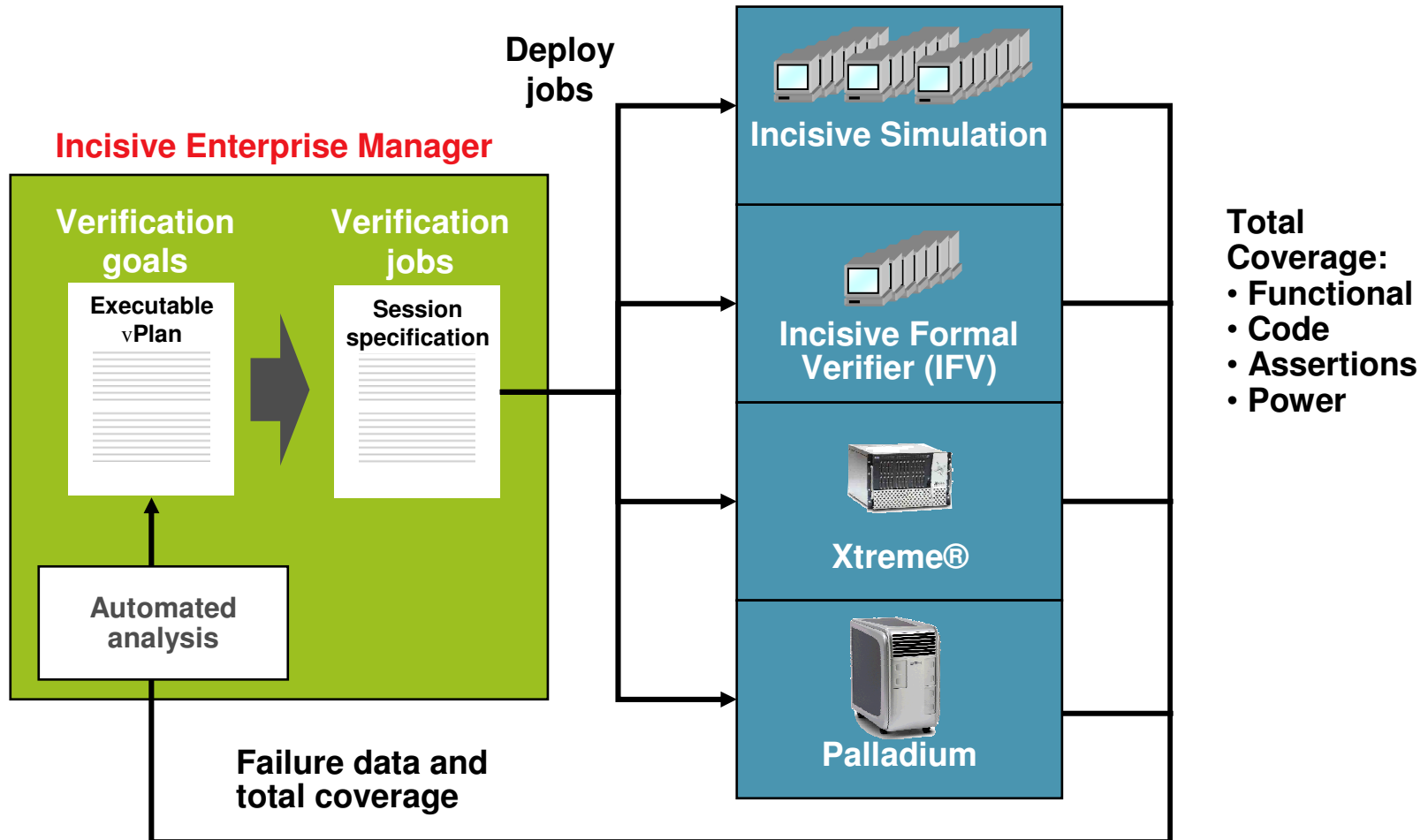
- Multiple I/O methodology support
 - Area or peripheral I/O
- Concurrent opt of I/O and core
- Congestion analysis/ route feasibility and “what-if” analysis
- Automatic RDL and 45° routing
- >40 customer tapeouts

“Encounter’s automated RDL routing for flip chip helped us meet our demanding schedule. It was by far most powerful solution to help us meet our demanding goals.” **Gopal Raghavan, CTO** 

“The Encounter system works perfectly on our Standard Design Platform (SDP) and special I/Os, and it helped us accelerate our flip chip design process.” **Nianfeng Li, VP Design** 



Incisive Enterprise Manager for verification engineers



Conformal Low Power *Verify* Structural, Rule, and Functional Checks – CPF Enabled

RTL/Logical Netlist

Level shifters

- Placement
- Location
- Connectivity

Isolation cells

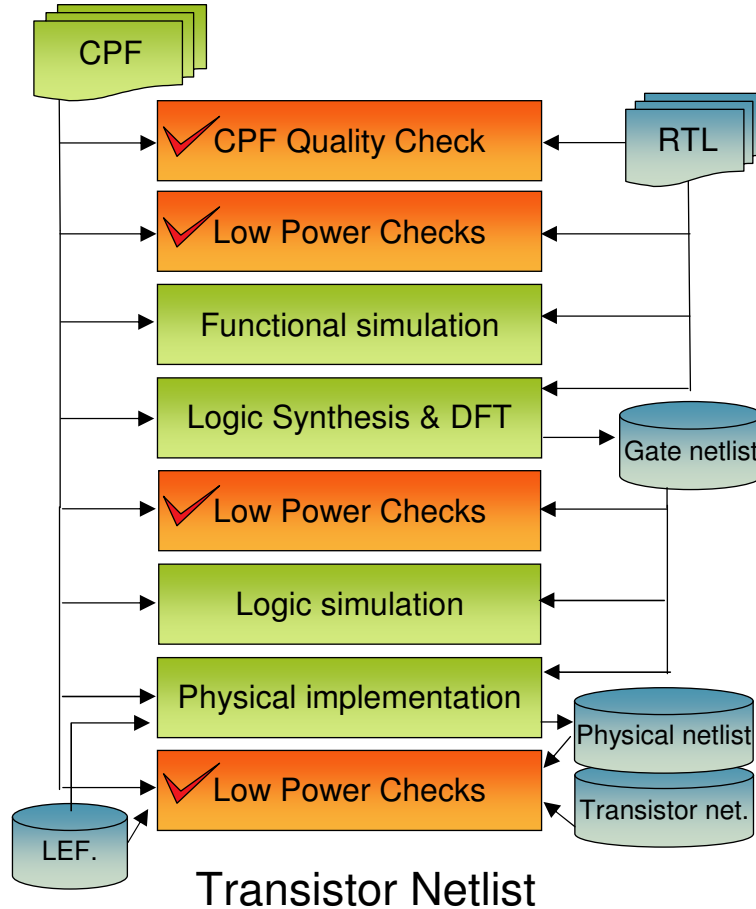
- Placement
- Isolation type
- Isolation function

State retention cells

- Placement
- Retention function

Miscellaneous

- Floating nets / pins
- Control Polarity



Transistor Netlist

- Transistor Stacking
- Un-buffered Input
- Macro Power Associations

Physical Netlist

Level shifters

- Placement/Location
- Power connectivity

Isolation cells

- Placement/type
- Power connectivity
- Isolation function

State retention cells

- Placement
- Power connectivity
- Retention function

Power and Ground Switch

- Power/Ground Connectivity
- Enable Control Polarity

Miscellaneous

- Shorts b/n VDD/VSS
- Always-on buffers

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Cadence VCAD

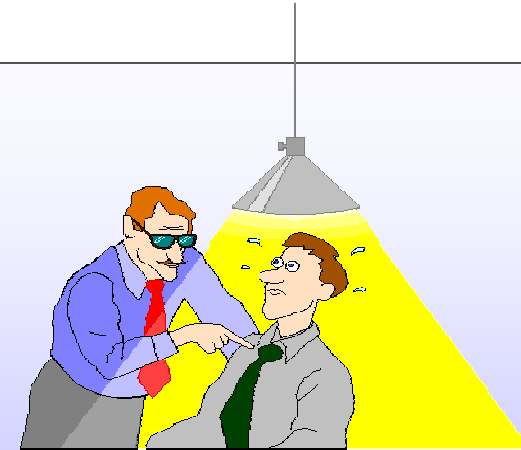


Дизайн-центр

Помещение



Оборудование

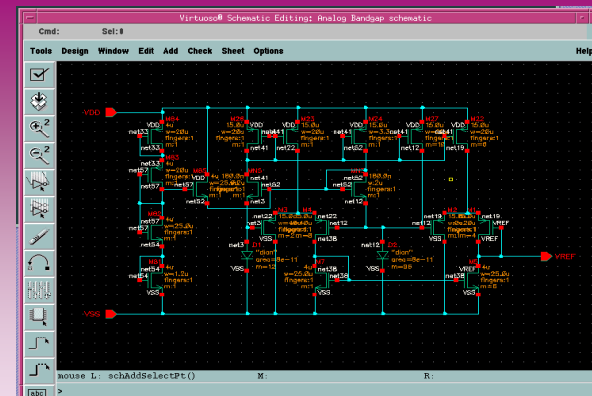


Разработчики

Cadence VCAD

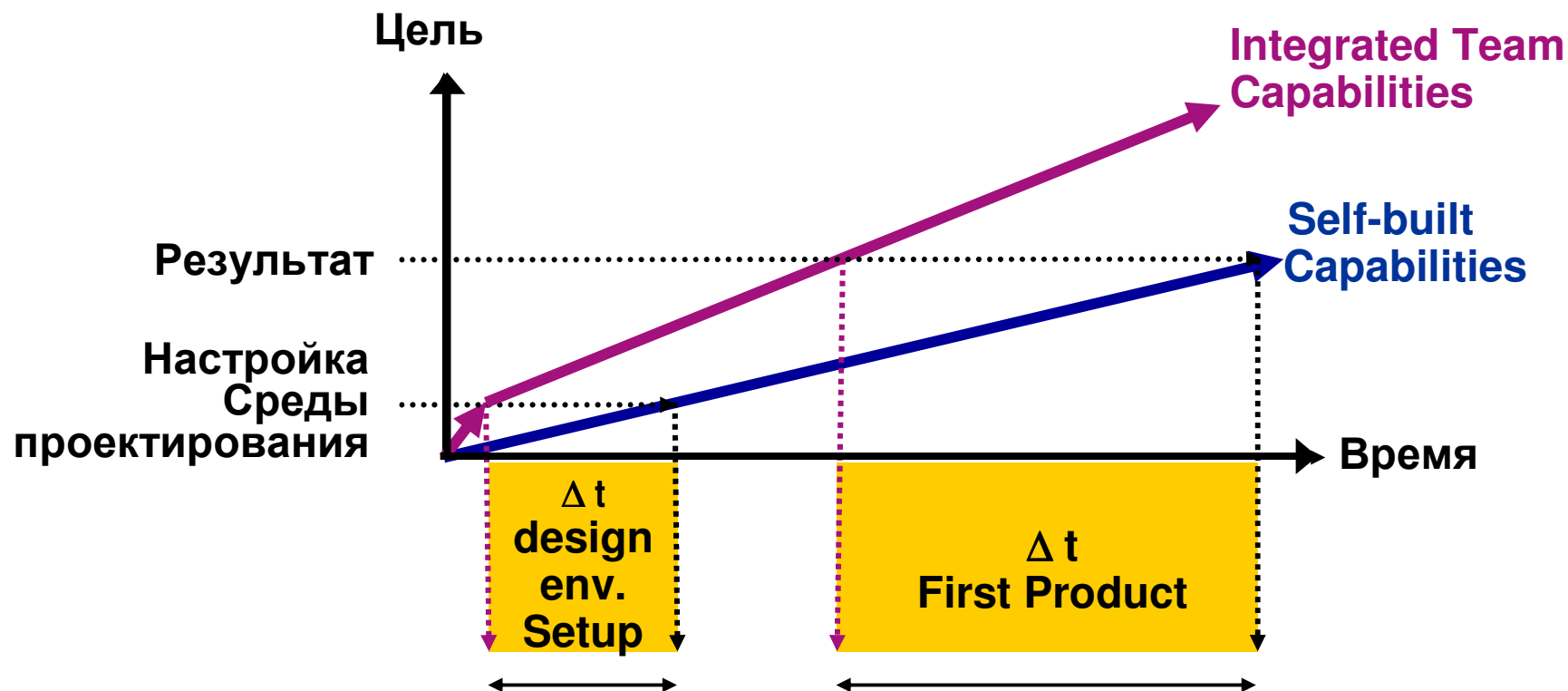


Среда проектирования и
поддержка



Ведение проекта

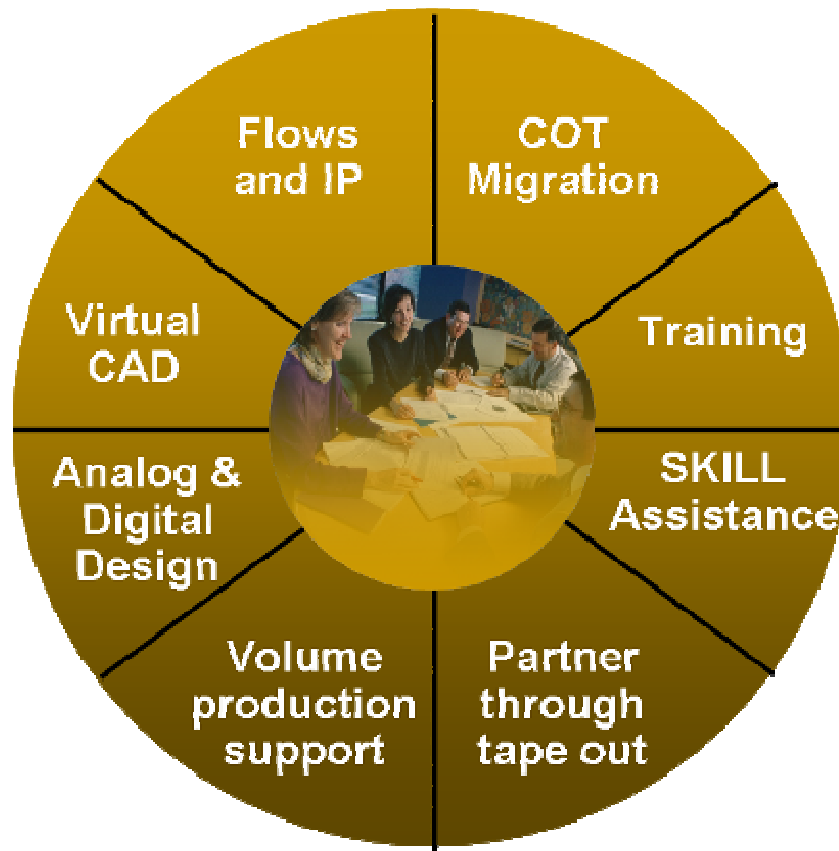
Cadence VCAD: преимущества сервисных услуг



- Экономия времени
- Оптимизация затрат
- Снижение рисков

Обширный набор сервисных услуг

Проверенные маршруты и методологии проектирования



Проектирование за 1 проход

Профессиональные услуги в области разработки и IP

Cadence, VCAD service.

- VCAD 65nm experience:
 - Short design info:
 - - 65nm technology
 - - main clock frequency 438MHz (worst corner)
 - - ~16M placeable instances
 - - 12 metal layers
 - - flip-chip design w/ 4440 bumps, die size 14.9x14.9mm²
 - - 6 partitions (3 partitions with master and one clone, 1 partition with master and three clones)
 - - few hundred of RAMs, few analog IPs

Major challenges for 65nm compare to 90nm:

1. Timing analysis: need to make more timing and RC corner analysis for Setup and especially for Hold.
2. Litho-Analysis and CMP-analysis – should be done, at least once for 65nm. VCAD offer is to run these checks on our side, just to make sure that everything is fine.
3. Power should be considered: Power-aware Timing/SI (skew/jitter/setup/hold) including Chip-package effects.
4. Low Power aspects should be simulated in analog simulator.
5. Very high-speed design below 90nm should go through dynamical power analysis, using correct and robust VCD/activity file.

Questions?

